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RM-6469

B. E. II (Sem. IV) (Comp.) Examination

May / June – 2010

Digital Electronics

Time : **3** Hours] [Total Marks : **100**

Instruction :

(1)

નીચે દર્શાવેલ ☛ નિશાનીવાળી વિગતો ઉત્તરવહી પર અવશ્ય લખવી.
Fillup strictly the details of ☛ signs on your answer book.

Name of the Examination :

☛ **B. E. 2 (Sem. 4) (Comp.)**

Name of the Subject :

☛ **Digital Electronics**

☛Subject Code No. : **6 4 6 9** ☛Section No. (1, 2,.....) : **1&2**

Seat No. :

Student's Signature

(2) Attempt **all** questions.
(3) Assume suitable data wherever **necessary**.
(4) Figures to the **right** indicate full marks.
(5) Draw logic circuit for design problem.
(6) Write both the sections in separate answer sheets.

SECTION - I

1 (a) Do as directed : **10**

(1) Define : Combinational circuit.
(2) Find the radix for the given number system :
(i) 1234 + 5432 = 6666
(ii) 33 ÷ 3 = 11.
(3) (4057.06)8 = (?)10.
(4) What is gray code ?
(5) Derive XNOR gate by using NAND gate.

(b) Explain 4 bit full adder with look ahead carry. 8

2 (a) Reduce the expression : **7**

(i) $A\left[B+\overline{C}\ \left(\overline{AB+A\overline{C}}\right)\right]$

(ii) $\left(\overline{A+\overline{BC}}\right)\left(A\overline{B}+ABC\right)$.

(b) Design BCD adder. **7**

OR

2 (a) Reduce the expression : 7

(i) $(B + BC)(B + \overline{B}C)(B + D)$

(ii) $A + B\left[AC + (B + \overline{C})D\right]$.

(b) Explain 'priority encoder'. 7

3 Any **three** : 18

(1) Design a combinational circuit using ROM. The ckt accepts a 3-bit number and generates an output binary number equal to the square of the input number.

(2) Implement the following function with a multiplexer.

$F(A, B, C, D) = \sum(0, 1, 3, 4, 8, 9, 15)$.

(3) Implement the following function with NAND gates :

$F(x, y, z) = \sum(0, 6)$.

(4) Design full adder circuit.

SECTION - II

4 (a) Answer the following : 10

(1) A _____ is a digital circuit which selects one of the n data inputs and routes it to the output :
(a) Multiplexer (b) Encoder
(c) Decoder.

(2) A 1 : 4 demux has _____ input and _____ outputs.
(a) 1, 4 (b) 4, 1
(c) 2, 4

(3) The _____ circuits do not use any memory.
(a) combinational (b) sequential
(c) hybrid

(4) The data stored by the memory element at any given instance of time is called as the _____ state of the sequential circuit.
(a) Next (b) Present
(c) Lost.

(5) The circuit that responds to the level of the input signal is called as _____ circuit.
(a) Level triggered (b) Edge triggered
(c) Pulse triggered

(6) An FF can store _____ bits.
(a) 1 (b) 2
(c) 3.

(7) If the data enter in a one bit at a time manner than it is called as _____ form.
(a) serial (b) parallel.

(8) In general the number of states = _____ where n is equal to the number of flip - flops.

(a) $1/2^n$ (b) 2^n

(c) $\log 2^n$

(9) Ring counter is _____ type counter.
(a) Synchronous (b) Asynchronous
(c) Ripple.

(10) A 4-bit binary counter is MOD _____ counter.
(a) 4 (b) 6
(c) 15.

(b) Convert the following : **10**
(1) SR flip flop to T flip-flop
(2) Flip flop to SR flip-flop.

5 (a) For the clocked JK flip-flop write the state table, draw the state diagram and write the state equation. **8**

(b) Explain 4-bit BCD Ripple counter, with timing diagram. **7**

OR

5 (a) Implement the following function using 16 : 1 multiplexer : **8**

$F(A, B, C, D, E) = \sum m(2, 4, 5, 7, 10, 14, 15, 16, 17, 25, 26, 30, 31)$.

(b) For the clocked D FF write the state table, draw the state diagram and write the state equation. **7**

6 (a) Design a counter that has a repeated sequence of six states as 000, 001, 010, 100, 101, 110. **7**

(b) Explain register with parallel load. **8**

OR

6 (a) Design a serial adder using a sequential-logic procedure. **7**

(b) Explain Johnson counter with timing diagram. **8**